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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MARK A. BURNS

Serial No. 10/026,053 (TI-33380)

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For: PARALLEL INTEGRATED CIRCUIT TEST APPARATUS AND TEST METHOD

Art Unit 2829

Examiner Jimmy Nguyen

Customer No. 23494

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4/21/04

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 33, all of the rejected claims. No claims have been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was filed after final rejection and was entered for purposes of appeal.

SUMMARY OF INVENTION

The invention relates to an apparatus for testing at least one first integrated circuit (IC) and at least one second IC using a single handler (304) coupled to a plurality of different testers (308, 336) for the first and second ICs. A first tester (308) is adapted to test the at least one first IC with a first test procedure and a second tester (336) is adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure. The first and second test procedures are adapted to test at least some different IC parameters with the first tester coupled to the second tester (Figs. 6-8). The first tester is adapted to calibrate the second tester and vice versa.(page 14, line 9ff) and at predetermined time intervals or when ambient temperature has changed by a predetermined amount. Data can be transmittable from the first tester to the second tester and/or from the second tester to the first tester (page 14, lines 1 to 6). A multiplexer can be coupled to the first and second testers, the multiplexer being adapted to multiplex the first and second test procedures on the first and second IC's (page 16, lines 5-6). The first tester can be indirectly coupled to the second tester by a host computer or host network.

ISSUE

The issue on appeal is whether claims 1 to 33 are anticipated by Maeng (U.S. 6,313,652).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

Claims 1 to 33 were rejected under 35 U.S.C. 102(e) as being anticipated by Maeng (U.S. 6,313,652). The rejection is again respectfully traversed.

It is fundamental that a rejection under section 102 requires that each and every feature of a claim as well as each and every function recited by the claimed features be found in a single reference. This is not the case with the subject rejection as is readily apparent not only as to the independent claims, but also as to the dependent claims wherein it is stated that the specific feature or features of the dependent claim is also not taught by Maeng.

Claim 1 requires that the first tester be coupled to the second tester.

Claim 1 requires, for example, a single handler *coupled* to the first and second testers. Even assuming, without agreement, that the transferring member 40 be a handler, the transferring member of Maeng is not coupled to first and second testers. In fact, the transferring member 40 doesn't appear to be coupled to anything in figure 4.

Claims 2 to 17 depend from claim 1 and therefore define patentably over Maeng for at least the reasons presented above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring that the first tester be adapted to calibrate the second tester. No such feature is found in Maeng either alone or in the combination as claimed. Considering the fact that the rejection is under section 102, the Examiner was requested to show where this features as well as features of

subsequent claims were to be found in Maeng, however no response to the requested has been provided.

Claim 3 further limits claim 2 by requiring that the second tester be adapted to submit a request for calibration to the first tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 4 further limits claim 2 by requiring that the first tester be adapted to calibrate the second tester at predetermined time intervals or when ambient temperature has changed by a predetermined amount. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 5 further limits claim 1 by requiring that the first test procedure comprise at least one of static and dynamic current and voltage tests, dynamic functional AC/DC tests, DC offset tests, AC timing relation tests, internal AC parametric tests, power supply current tests, leakage current tests, gain tests, and/or low speed digital pattern tests; and wherein the second test procedure comprises at least one of external AC parametric tests, signal-to-noise ratio tests, DSP-based AC tests, distortion tests, thermal soaks, RF tests, and/or high speed digital pattern tests with precision timing. No such combination is taught or suggested by Maeng.

Claim 6 further limits claim 1 by requiring that data be transmittable from the first tester to the second tester and/or from the second tester to the first tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 7 further limits claim 1 by requiring a multiplexer coupled to the first and second testers, wherein the multiplexer is adapted to multiplex the first and second test procedures on the first and second IC's.

Claim 8 further limits claim 7 by requiring that the first and second IC's be in die form integral to a single wafer, wherein the apparatus further comprises a wafer probe simultaneously coupleable to the first and second IC's. No such combination is taught or suggested by Maeng.

Claim 9 further limits claim 1 by requiring that the first and second testers comprise low cost testers. No such combination is taught or suggested by Maeng.

Claim 10 further limits claim 1 by requiring that the first and second testers comprise high cost testers. No such combination is taught or suggested by Maeng.

Claim 11 further limits claim 1 by requiring that first IC's that fail the first test procedures be moved to the second tester for testing with the second test procedure. No such combination is taught or suggested by Maeng.

Claim 12 further limits claim 1 by requiring control circuitry coupled to the first tester and second tester and storage means coupled to the control circuitry, first tester and second tester. No such combination is taught or suggested by Maeng.

Claim 13 further limits claim 12 by requiring that first and second IC test procedure result information be storable in the storage means with respect to first and second IC position. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 14 further limits claim 12 by requiring that the first and second IC's store identification information, wherein first and second IC test procedure result information is storable in the storage means with respect to the first and second IC identification information. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 15 further limits claim 1 by requiring that the apparatus be adapted to test the at least one first IC with the first tester first test procedure simultaneously while the at least one second IC is tested with the second tester second test procedure. No such combination is taught or suggested by Maeng.

Claim 16 further limits claim 1 by requiring that the first tester be indirectly coupled to the second tester by a host computer or host network. No such combination is taught or suggested by Maeng.

Claim 17 further limits claim 1 by requiring that the first tester be integral to the second tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 18 requires, among other features, a single handler coupled to the first and second testers, the first and second test procedures adapted to test at least some different IC parameters. The argument presented above with reference to claim 1 applies as well to this claim.

Claim 18 further requires a first environmental chamber coupled to the first tester and a second environmental chamber coupled to the second tester, wherein the first and second test procedures comprise subjecting the first and second IC's to different environmental tests. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 19 requires, among other features, a single handler coupled to the first and second testers, wherein the first and second test procedures are adapted to test at least some different IC parameters, and wherein the first tester is integral to the handler. The argument presented above with reference to claim 1 applies as well to this claim.

Claim 20 depends from claim 19 and therefore defines patentably over Maeng for at least the reasons presented above with reference to claim 19.

Claim 21 requires, among other features, the step of coupling the first tester to the second tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claims 22 to 33 depend from claim 21 and therefore define patentably over Maeng for at least the reasons presented above with reference to claim 21.

Claim 22 further limits claim 21 by requiring the step of calibrating the second tester with the first tester and/or calibrating the first tester with the second tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 23 further limits claim 22 by requiring that the calibrating be in response to a request for calibration from the first or second tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 24 further limits claim 22 by requiring that the first tester be adapted to calibrate the second tester at predetermined time intervals or when ambient temperature has changed by a predetermined amount. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 25 further limits claim 21 by requiring the step of transmitting data from the first tester to the second tester and/or transmitting data from the second tester to the first tester. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 26 further limits claim 21 by requiring that the first test procedure comprise at least one of static and dynamic current and voltage tests, dynamic

functional AC/DC tests, DC offset tests, AC timing relation tests, internal AC parametric tests, power supply current tests, leakage current tests, gain tests, and/or low speed digital pattern tests; and wherein the second test procedure comprises at least one of external AC parametric tests, signal-to-noise ratio tests, DSP-based AC tests, distortion tests, thermal soaks, RF tests, and/or high speed digital pattern tests with precision timing. No such combination is taught or suggested by Maeng.

Claim 27 further limits claim 21 by requiring the step of multiplexing the first and second test procedures on the first and second IC's. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 28 further limits claim 27 by requiring that the first and second IC's be in die form integral to a single wafer, wherein the method further comprises coupling a wafer probe simultaneously coupleable to the first and second IC's to perform the first and second test procedures. No such combination is taught or suggested by Maeng.

Claim 29 further limits claim 21 by requiring the steps of subjecting the first IC's to a first environmental test while performing the second test procedure and subjecting the second IC's to a second environmental test while performing the first test procedure, wherein the first environmental test is different from the second environmental test. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 30 further limits claim 21 by requiring the step of moving first IC's that fail the first test procedures to the second tester for testing with the second test procedure. No such combination is taught or suggested by Maeng.

Claim 31 further limits claim 21 by requiring the step of storing the first and second IC test procedure result information with respect to first and second IC position. No such combination is taught or suggested by Maeng.

Claim 32 further limits claim 21 by requiring the step of storing the first and second IC test procedure result information with respect to the first and second IC identification information. No such feature is found in Maeng either alone or in the combination as claimed.

Claim 33 further limits claim 21 by requiring the step of simultaneously testing the second IC with the second test procedure while testing the first IC with the first test procedure. No such combination is taught or suggested by Maeng.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

1. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure;

a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure, wherein the first and second test procedures are adapted to test at least some different IC parameters, wherein the first tester is coupled to the second tester; and

a single handler coupled to the first and second testers.

2. The apparatus according to Claim 1, wherein the first tester is adapted to calibrate the second tester.

3. The apparatus according to Claim 2, wherein the second tester is adapted to submit a request for calibration to the first tester.

4. The apparatus according to Claim 2, wherein the first tester is adapted to calibrate the second tester at predetermined time intervals or when ambient temperature has changed by a predetermined amount.

5. The apparatus according to Claim 1, wherein the first test procedure comprises at least one of static and dynamic current and voltage tests, dynamic functional AC/DC tests, DC offset tests, AC timing relation tests, internal AC parametric tests, power supply current tests, leakage current tests, gain tests, and/or low speed digital pattern tests; and wherein the second test procedure comprises at least one of external AC parametric tests, signal-to-noise ratio tests, DSP-based AC tests, distortion tests, thermal soaks, RF tests, and/or high speed digital pattern tests with precision timing.

6. The apparatus according to Claim 1, wherein data is transmittable from the first tester to the second tester and/or from the second tester to the first tester

7. The apparatus according to Claim 1, further comprising a multiplexer coupled to the first and second testers, wherein the multiplexer is adapted to multiplex the first and second test procedures on the first and second IC's.

8. The apparatus according to Claim 7, wherein the first and second IC's are in die form integral to a single wafer, wherein the apparatus further comprises a wafer probe simultaneously coupleable to the first and second IC's.

9. The apparatus according to Claim 1, wherein the first and second testers comprise low cost testers.

10. The apparatus according to Claim 1, wherein the first and second testers comprise high cost testers.

11. The apparatus according to Claim 1, wherein first IC's that fail the first test procedures are moved to the second tester for testing with the second test procedure.

12. The apparatus according to Claim 1, further comprising:

control circuitry coupled to the first tester and second tester; and

storage means coupled to the control circuitry, first tester and second tester.

13. The apparatus according to Claim 12, wherein first and second IC test procedure result information is storable in the storage means with respect to first and second IC position.

14. The apparatus according to Claim 12, wherein the first and second IC's store identification information, wherein first and second IC test procedure result information is storable in the storage means with respect to the first and second IC identification information.

15. The apparatus according to Claim 1, wherein the apparatus is adapted to test the at least one first IC with the first tester first test procedure simultaneously while the at least one second IC is tested with the second tester second test procedure.

16. The apparatus according to Claim 1, wherein the first tester is indirectly coupled to the second tester by a host computer or host network.

17. The apparatus according to Claim l, wherein the first tester is integral to the second tester.

18. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure;

a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure;

a single handler coupled to the first and second testers; wherein the first and second test procedures are adapted to test at least some different IC parameters;

a first environmental chamber coupled to the first tester; and

a second environmental chamber coupled to the second tester, wherein the first and second test procedures comprise subjecting the first and second IC's to different environmental tests.

19. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure; a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure; and

a single handler coupled to the first and second testers, wherein the first and second test procedures are adapted to test at least some different IC parameters, and wherein the first tester is integral to the handler.

20. The apparatus according to Claim 19, wherein the second tester is integral to the handler.

21. A method of testing at least one first integrated circuit (IC) and at least one second IC in an apparatus comprising a first tester and a second tester coupled to a single handler, the method comprising:

coupling the first tester to the second tester;

testing the first IC with a first test procedure using the first tester; and testing the second IC with the first test procedure simultaneously while testing the first IC's with a second test procedure using the second tester, wherein testing IC's with the first test procedure comprises testing at least some different IC parameters than testing IC's with the second test procedure.

22. The method according to Claim 21, further comprising calibrating the second tester with the first tester and/or calibrating the first tester with the second tester.

23. The method according to Claim 22, wherein the calibrating is in response to a request for calibration from the first or second tester.

24. The method according to Claim 22, wherein the first tester is adapted to calibrate the second tester at predetermined time intervals or when ambient temperature has changed by a predetermined amount.

25. The method according to Claim 21, further comprising transmitting data from the first tester to the second tester and/or transmitting data from the second tester to the first tester.

26. The method according to Claim 21, wherein the first test procedure comprises at least one of static and dynamic current and voltage tests, dynamic functional AC/DC tests, DC offset tests, AC timing relation tests, internal AC parametric tests, power supply current tests, leakage current tests, gain tests, and/or low speed digital pattern tests; and wherein the second test procedure comprises at least one of external AC parametric tests, signal-to-noise ratio tests, DSP-based AC tests, distortion tests, thermal soaks, RF tests, and/or high speed digital pattern tests with precision timing.

27. The method according to Claim 21, further comprising multiplexing the first and second test procedures on the first and second IC's.

28. The method according to Claim 27, wherein the first and second IC's are in die form integral to a single wafer, wherein the method further comprises coupling a wafer probe simultaneously coupleable to the first and second IC's to perform the first and second test procedures.

29. The method according to Claim 21, further comprising:

subjecting the first IC's to a first environmental test while performing the second test procedure; and

subjecting the second IC's to a second environmental test while performing the first test procedure, wherein the first environmental test is different from the second environmental test.

30. The method according to Claim 21, further comprising moving first IC's that fail the first test procedures to the second tester for testing with the second test procedure.

31. The method according to Claim 21, further comprising storing the first and second IC test procedure result information with respect to first and second IC position.

32. The method according to Claim 21, further comprising storing the first and second IC test procedure result information with respect to the first and second IC identification information.

33. The method according to Claim 21, further comprising simultaneously testing the second IC with the second test procedure while testing the first IC with the first test procedure.